***Advanced System on Chip Course***

**QUIZ 8**

**Issue 1.0**

# MODULE 8: AXI UART and AXI4-Stream Peripheral

**Question 1:**

Which of the following tasks is typically performed by a UART peripheral?

1. It manages the data flow between a system bus (e.g. AXI) and a monitor.
2. It transforms data from serial to parallel.
3. It provides interface for I2C and SPI serial communications.
4. It generates the system clocking signal.

**Question 2:**

Which of the following statements expresses an advantage of serial data transmission over parallel data transmission?

1. Serial transmission provides higher data throughputs at the same clock rate.
2. Serial transmission is more vulnerable to noise.
3. Serial transmission requires fewer wiring overheads.
4. Serial transmission is always more power efficient.

**Question 3:**

Why are synchronous serial links considered more reliable than synchronous parallel channels?

1. Because parallel channels are vulnerable to errors caused by crosstalk noise between parallel data lines.
2. Because parallel channels are vulnerable to errors caused by variations in power supply.
3. Because parallel channels are vulnerable to errors caused by synchronization failures caused by clock jitter.
4. All of the above.

**Question 4:**

Which of the following statements is correct?

1. Synchronous communication schemes use a clock signal to coordinate data transmission between sender and receivers; such coordination is not needed in asynchronous communication technique.
2. Asynchronous communication schemes use a clock signal to coordinate data transmission between a sender and a receiver; such coordination is not needed in synchronous communication techniques.
3. Asynchronous communication schemes use a clock signal to coordinate data transmission between a sender and a receiver, while synchronous communication techniques use extra bits to synchronize data transmission.
4. Synchronous communication schemes use a clock signal to coordinate data transmission between a sender and a receiver, while asynchronous communication techniques use extra bits to synchronize data transmission.

**Question 5:**

Which of the following statements is correct?

1. The communication between two UART devices is typically synchronous with pre-agreed data transmission rate.
2. The communication between two UART devices is typically synchronous, wherein the data transmission rate is controlled only by the clock frequency of the sender.
3. The communication between two UART devices is asynchronous, wherein the data transmission rate is fixed.
4. The communication between two UART devices is asynchronous, wherein the data transmission rate can continuously vary.

**Question 6:**

The frequency of the Baud clock depends on the following factors:

1. The frequency of the System on Chip clock.
2. The target data transmission rate at the output of the UART transmitter.
3. The configuration of the Baud generator (divisor).
4. All of the above.

**Question 7:**

Which of the following is NOT a task of the UART receiver?

1. Receiving data information at a rate specified by the clock generated from the Baud generator.
2. Converting data from parallel to serial.
3. Writing the received byte to the receiver FIFO.
4. Storing data temporarily in a shift register.

**Question 8:**

Why does a UART controller typically have a FIFO register connected to its transmitter?

1. To convert between the high frequency of the transmitting system and the low data rate of the communication channel.
2. To temporarily store data to be transmitted in order to improve system efficiency.
3. To convert between the low frequency of the transmitting system and the high data rate of the communication channel.
4. To give the host system more time to handle an interrupt from the UART.

**Question 9:**

AXI-4 stream protocol:

1. can be used to connect only one manager, that generates stream data, to one or various subordinates, that receive stream data.
2. can be used to connect only one manager, that generates stream data, to only one subordinate, that receives stream data.
3. can be used to connect one or various managers, that generate stream data, to one or various subordinates, that receive stream data.
4. can be used to connect one or various managers, that generates stream data, to only one subordinate, that receives stream data.

**Question 10:**

The AXI4-stream protocol is a used as a standard interface for:

1. byte stream transmissions.
2. continuous aligned stream transmissions.
3. continuous unaligned aligned stream transmissions.
4. All of the above. AXI-Stream is not constrained to any data stream type.

**Question 11:**

Which of the following statements is true?

1. A Transfer is a group of bytes that are transported together across an AXI4-Stream interface.
2. A Packet is the highest level of byte grouping in an AXI4-Stream.
3. A Frame is the highest level of byte grouping in an AXI4-Stream. A frame contains an integer number of packets.
4. A Frame is a group of bytes that are transported together across an AXI4-Stream interface.

**Question 12:**

A continuous alignment stream is:

1. The transmission of a number of data bytes where every packet has no position or null bytes.
2. The transmission of a number of data bytes where there are no position bytes between the first data byte and the last data byte.
3. The transmission of a number of data bytes and position bytes.
4. The transmission of a number of data and null bytes.

**Question 13:**

The manager signals in the simplest AXI4-stream mechanism are:

1. TVALID, TLAST, and TUSER.
2. TVALID, TLAST, TDATA, and TUSER.
3. TLAST, TDATA, and TUSER.
4. TVALID, TLAST, TDATA, and TREADY.

**Question 14:**

The signal TUSER in the AXI4-Stream protocol:

1. identifies the destination (subordinate) of a Transfer.
2. indicates the boundary of a packet.
3. is user-defined sideband information that can be transmitted alongside the data stream.
4. indicates that the subordinate can accept a transfer in the current cycle.

**Question 15:**

In the AXI4-Stream handshake protocol:

1. Transfer can take place in any cycle between a TVALID deassertion and TREADY assertion.
2. Transfer can take place in any cycle between a TVALID assertion and TREADY assertion.
3. Transfer can take place in any cycle between a TVALID deassertion and TREADY deassertion.
4. Transfer takes place in the cycle that TVALID and TREADY are both asserted.

**Answers**

Q1) 2

Q2) 3

Q3) 1

Q4) 4

Q5) 3

Q6) 4

Q7) 2

Q8) 2

Q9) 3

Q10) 4

Q11) 3

Q12) 1

Q13) 2

Q14) 3

Q15) 4