***Advanced System on Chip Course***

**QUIZ 2**

**Issue 1.0**

# MODULE 2: Arm and Arm Processors

**Question 1:**

What does Arm Ltd produce?

1. Arm mainly produces microprocessor chips based on the RISC architecture.
2. Arm is an IP company that mainly offers processor IPs, various other physical IPs, development tools, and support for his products.
3. Arm is an IP company that offers various RISC and CISC processors aimed at embedded applications.
4. Arm is an IP company that mainly fabricates microprocessor and graphic processor chips.

**Question 2:**

The Cortex-A processors are

1. Low cost processors for deterministic microcontroller applications.
2. High-performance processors for real-time applications with high reliability requirements.
3. High-performance processors for open Operating Systems.
4. Low-power processors for high security applications.

**Question 3:**

The Cortex-A series family include

1. Processors with 16-bit and 32-bit CPUs.
2. Processors with 8-bit, 16-bit, and 32-bit CPUs.
3. Processors with 32-bit, and 64-bit CPUs.
4. Only processors with 32-bit CPUs.

**Question 4:**

Which of the following statements is correct?

1. All Cortex-A processors are Armv7 architecture.
2. All Cortex-M processors are Armv7 architecture.
3. All Cortex processors are Armv7 architecture.
4. All Armv7-A architecture processors are Cortex-A processors.

**Question 5:**

What is the ThumbEE instruction set?

1. It is a Thumb-based instruction set with some changes to make it a better target for dynamically generated code.
2. It is just another name to refer to the Thumb-2 when applied to the Armv7 architecture.
3. It is a Thumb-based instruction set which is defined for the Armv7-R architecture and aimed to guarantee real-time operations.
4. It is a Thumb-based instruction previous to the Thumb-2 technology that was defined for the Armv5 architecture and which is now superseded.

**Question 6:**

What is the best definition for the Thumb-2 instruction set?

1. Unlike the Arm instruction set, which is 16-bit, Thumb-2 is a 32-bit instruction set that is a superset of the previous Arm instruction set to provide better performance.
2. Unlike the Arm instruction set, which is 32-bit, Thumb-2 is a 16-bit instruction set that is a subset of the previous Arm instruction set to provide better code density.
3. Like the Arm instruction set, which is 32-bit, Thumb-2 is a 32-bit instruction set that is a subset of the previous Arm instruction to provide better code density.
4. Unlike the Arm instruction set, which is 32-bit, Thumb-2 is a combination of 16-bit and 32-bit instructions that is a subset of the previous Arm instruction set that achieves almost the same performance at a better code density.

**Question 7:**

The Armv7 architecture

1. is based on the Arm (A32) instruction set.
2. is based on the Thumb-1 instruction set.
3. is based on the Thumb-2 and the ThumbEE instruction sets, and does not support the Arm (A32) instruction set.
4. is based on the Thumb-2 and the ThumbEE instruction sets, but does support the Arm (A32) instruction set as well.

**Question 8:**

In the AAPCS of the ARMv7-A

1. the first four registers r0-r3 (which are called a1-a4) are used to pass argument values into a subroutine and to return a result value from a function.
2. the first four registers r0-r3 (which are named a1-a4) are used to pass argument values into a subroutine and registers r4-r7 (which are named a5-a8) are used to return a result value from a function.
3. the first four registers r0-r3 (which are called v1-v4) are used to hold the values of a routine’s local variables.
4. registers r4-r7 (which are named a1-a4) are used to hold the values of a routine’s local variables..

**Question 9:**

 Which of the following statements is correct?

1. Armv7-A has seven basic operating modes, each having access to its own stack space and share a common set of registers.
2. Armv7-A has seven basic operating modes, four of these being “exception” modes with a different subset of registers and three being “normal” modes with a common set of registers but different privilege levels.
3. Armv7-A has seven basic operating modes, each having access to its own stack space and a different subset of registers.
4. Armv7-A has seven basic operating modes, five of these being privileged and two unprivileged modes.

**Question 10:**

The term ‘memory type’ in ARMv7 processors

1. refers to the three memory technologies (ROM, SRAM, or DRAM) available in Arm processors and to their respective access rules.
2. refers to the most significant memory attribute specified for each memory region (Normal, Device or Strongly-ordered) and to their respective access rules.
3. refers to the set of memory attributes (shareability, cacheability etc.) defined for each memory region
4. refers to the various memory regions defined in the memory map of the architecture.

**Question 11:**

In the ARMv7-A, the mapping of instruction memory is

1. big-endian but can be configured as little-endian at the system level.
2. always big-endian.
3. little-endian but can be configured as big-endian at the system level.
4. always little-endian.

**Question 12:**

 In the Armv7 architecture with Virtualization Extension

1. a new hypervisor (Hyp) mode is introduced, which is a Non-secure but highly privileged mode that enables to run a hypervisor responsible to switching guest operating systems.

2. a new hypervisor (Hyp) mode is introduced, which is a secure and highly privileged mode that enables to run a hypervisor responsible to switching guest operating systems running in the normal mode.

3. the hypervisor responsible to switching guest operating systems runs in the privileged System mode, which is Non-secure.

4. all operating systems must run in a secure-mode.

**Question 13:**

Cortex-A9 MPCores

1. contain up to 6 Cortex-A9 processors with shared data caches and independent instruction caches.
2. contain up to 4 Cortex-A9 processors with shared data caches and independent instruction caches.
3. contain up to 4 Cortex-A9 processors with independent data and instruction caches.
4. contain up to 6 Cortex-A9 processors with shared instruction caches and independent data caches.

**Question 14:**

The SCU unit is necessary in multiprocessor Cortex-A9 cores

1. to interconnect the CPU register set of all A9 processors thorough an internal shared data bus.
2. to connect all A9 processors to the memory system, maintain LI data cache coherency and arbitrate requesting L2 accesses.
3. to arbitrate the requests of the CPUs of all A9 processors to access the shared Neon/FPU unit, if implemented.
4. to arbitrate the requests of the CPUs of all A9 processors to access the shared L1 shared data cache through the AXI bus.

**Question 15:**

Neon technology is

1. the implementation of the Advanced SIMD extension available only in Cortex-A processors for efficiently process multimedia applications.
2. the implementation of the combination of the DSP extension and the Floating Point architecture (VFP) available only in Cortex-A processors.
3. an optional extension available for ARMv7-based Cortex processors to process floating point operations more efficiently.
4. a set of software libraries to speed up half-word vector computations .

**Answers**

Q1)2

Q2)3

Q3)3

Q4)4

Q5)1

Q6)4

Q7)4

Q8)1

Q9)3

Q10)2

Q11)4

Q12)1

Q13)3

Q14)2

Q15)1