***Advanced System on Chip Course***

**QUIZ 6**

**Issue 1.0**

# MODULE 6: AMBA AXI4 Bus Architecture

**Question 1:**

Which of the following tasks is NOT a function of the system bus?

1. Controlling the flow of data between the processor and the memory block.
2. Allowing information to be transferred between the processor and external peripherals.
3. Connecting the ALU unit to the register file.
4. Providing temporary buffer for control signals.

**Question 2:**

Which of the following characteristics of an SoC is typically affected by the design of its bus?

1. Performance.
2. Power consumption.
3. Reliability.
4. All of the above.

**Question 3:**

What is the need for communication standards?

1. To speed up the SoC design process.
2. To improve SoC performance.
3. To reduce SoC power consumption.
4. All of the above.

**Question 4:**

Which of the following descriptions of Arm AMBA is NOT correct?

1. AMBA is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in system-on-a-chip designs.
2. AMBA is one of the most widely used on chip bus standard architectures.
3. AMBA is technology-dependent.
4. AMBA promotes design reuse.

**Question 5:**

Which of the following AMBA bus families is used for low-bandwidth communication with peripherals?

1. AXI
2. AHB
3. APB
4. ATB

**Question 6:**

The AMBA AXI protocol:

1. uses common address/control and data phases, has separate read and write data channels, and does not support out-of-order transactions.
2. uses separate address/control and data phases, has separate read and write data channels, and does not support out-of-order transactions.
3. uses separate address/control and data phases, has a single common read and write data channel, and does support out-of-order transactions.
4. uses separate address/control and data phases, has separate read and write data channel, and does support out-of-order transactions.

**Question 7:**

AXI4-Lite is a light-weight variant of the AXI4 interface. Some restrictions that apply are:

1. Data bit-width is restricted to 16 bits, maximum clock frequency is lower, and all accesses are defined to be the data width.
2. Data bit-width is restricted to 16 bits, burst length is always 1, and all accesses are defined to be the data width.
3. Does not support AXI IDs, burst length is always 1, and all accesses are defined to be the data width.
4. maximum clock frequency is lower, burst length is always 1, and all accesses are defined to be the data width.

**Question 8:**

The AXI4-Stream protocol:

1. is a bidirectional protocol designed for stream data burst transfers up to 256 beats that supports a data bus width of 32-bit or 64-bit.
2. is a bidirectional protocol designed for stream data burst transfers up to 256 beats that allows the data width to be any integer number of data bytes.
3. is a unidirectional protocol designed for unlimited stream data burst transfers that allow the data width to be any integer number of data bytes.
4. is a unidirectional protocol designed for stream data burst transfers up to 256 beats that allows the data width to be any integer number of data bytes.

**Question 9:**

The AXI protocol is burst-based and defines the following transaction channels:

1. Read address, write address, read data, write data, and write response.
2. Read/write address, read data, write data, and write response.
3. Read/write address, read/write data, and write response.
4. Read/write address and read/write data.

**Question 10:**

The communication between manager and subordinate in the AXI4 protocol is performed by:

1. one-way handshaking (sender).
2. two-way handshaking (sender-receiver).
3. three-way handshaking (sender-receiver-sender).
4. four way handshaking (sender-receiver-sender-receiver).

**Question 11:**

In the AXI4 protocol, the LAST signal is used:

1. in the address and data read and write channels to indicate the transfer of the final data item in a transaction.
2. in the address read and write channels to indicate the transfer of the final data item in a transaction.
3. in the data read and write channels to indicate the transfer of the final data item in a transaction.
4. in the write response channels to indicate the transfer of the final data item in a transaction.

**Question 12:**

In the AXI4 protocol:

1. input signals are sampled on the rising edge of ACLK and output signal changes must occur after the rising edge of ACLK.
2. input signals are sampled on the falling edge of ACLK and output signal changes must occur after the rising edge of ACLK.
3. input signals are sampled on the rising edge of ACLK and output signal changes must occur after the falling edge of ACLK.
4. input signals are sampled on the falling edge of ACLK and output signal changes must occur after the falling edge of ACLK.

**Question 13:**

In the AXI4 protocol:

1. the reset signal is active-HIGH and must be asserted and deasserted synchronously.
2. the reset signal is active-LOW and must be asserted and deasserted synchronously.
3. the reset signal is active-HIGH and can be asserted asynchronously but must be deasserted synchronously.
4. the reset signal is active-LOW and can be asserted asynchronously but must be deasserted synchronously.

**Question 14:**

Regarding the AXI4 handshaking process:

1. Transfer occurs only when boththe VALID and READY signals are high.
2. Transfer occurs only when the VALID signal is high and the READY signal is low.
3. Transfer occurs only when the VALID signal is low and the READY signal is low.
4. Transfer occurs only when boththe VALID and READY signals are high.

**Question 15:**

Regarding the AXI4 handshaking process:

1. A source is permitted to wait until READY is asserted before asserting VALID.
2. A destination is NOT permitted to wait for VALID to be asserted before asserting the corresponding READY.
3. A source is NOT permitted to wait until READY is asserted before asserting VALID.
4. If READY is asserted, it is NOT permitted to deassert READY before VALID is asserted.

**Answers**

Q1)2

Q2)4

Q3)3

Q4)1

Q5)3

Q6)4

Q7)3

Q8)3

Q9)1

Q10)2

Q11)3

Q12)1

Q13)4

Q14)1

Q15)3